PLBD5EITO Specification

Version	Note	Date
V1.0	Create	2018/01/15
V1.1	Modify Module Outline	2018/04/13
V1.2	Only for PLBD5EITO	2018/08/03
V1.3	Add label information	2018/08/23
V1.4		2018/09/27
V1.5	Modify the Memory to Flash	2018/12/17
V1.6	Add Packing information	2021/01/13

Contents

1.Functional Characteristics

PLBD5EITO is SOC module developed based on the Bluetooth 5 standards. The internal integration architecture ARM® Cortex®-M0 processor and 8Mbit-SPI-FLASH.
It has the advantage of small volume, low power consumption, long distance transmission, strong anti-jamming capability, low cost.Specifically applied to Bluetooth low power control area,and suitable for various occasions short distance wireless communication.

PLBD5EITO integral compact, simplifies the design in hardware and institution for user. The module interface open completely to make the users has more flexible secondary development space.

The PLBD5EITO has a standard 2-wire uart interface (RX and TX) and has adjustable baud rates up to 1MPB. The PLBD5EITO integrates a universal asynchronous receiver/transmitter that support much of the functionality of the industry-standard 16550 UART. Both high and low baud rates can be supported by 16 MHz system clock. The PLBD5EITO UART operates correctly with the host UART as long as the combined baud rate error of the two devices is within ±5%.

1.1.Product feature

PLBD5EITO Supported AT Command Protocol, could be easily porting into different MCU controllers.
1: PLBD5EITO under Bluetooth 5 specification.
2: Very small current consumption.
3: Integrated 8Mbit FLASH Memory (Optional).Easy to extend SPI Flash.
4: Support OTA function.
5: “Near Field Mode” function @-20db RF.

1.2. Main Application domain.

1：MCU data pass-through.
2：Bluetooth Printer / Scanner / Digital price tag etc.
3：Remote control / Keyboard and Mouse / Toys / Smart phone self timer etc.
4：Industrial remote control / Industrial telemetry / Industrial data collection.
5：Smart home / Intelligent lighting / Intelligent access control system.

1.3. PLBD5EITO Certificate

PLBD5EITO has been certified by FCC/IC/MIC/RoHS. The certificate number as follow:

FCC ID : 2AQV6Buffalo-D5-FLASH

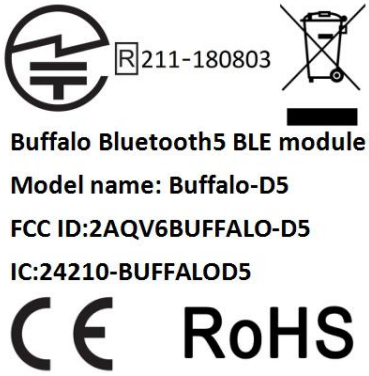
IC:24210-BUFFALOD5

MIC:211-180803

1.3.1. Label Information

A):Lable on Module

The label is attached to the module



B) :Label on Carton

The label is attached to the outer carton

2.Electrical Specification

- 64kB One-Time-Programmable (OTP) memory
- 96kB Data/Retention SRAM
- 128kB ROM
- 8Mbit FLASH
- Absolute Voltage:2.35V~3.60V
- Supply current at VBAT-3V: TX: 3.4 mA, RX: 3.7 mA (with ideal DC-DC)
- Deep Sleep Power:＜1uA
- RF Frequency:2400MHz ~ 2483.5 MHz
- Channel Spacing:2MHz
- Channel Center Frequency:2402MHz~2480MHz
- Modulation:GFSK
- -93 dBm receiver sensitivity @ BER<0.1％
- TX_POWER RANGE:-20dBm ~ +0dBm
- Operating Temperature:-40°C to +85°C

3.Peripheral Interface

- 2 x UART interface
- 1 x SPI interface
- 1 x I2C interface
- 15 x GPIOs
- 1 x 16-bit general purpose timer
- 1 x 14-bit general purpose timer
- 2 x 10-bit ADC
- 4 x PWM interface

4.Hardware design and PCB layout

4.1.Pin assignment and Pin description

PLBD5EITO Pin definition can refer to **Figure 2**.

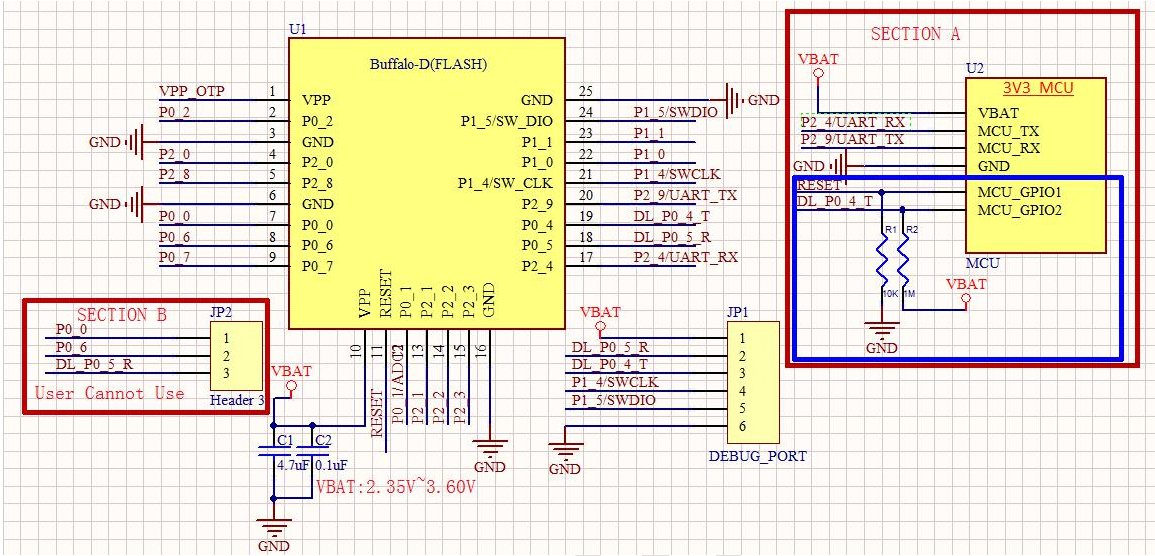
Table 1:Module Pin Description

Pin Number	*Pin Name*	*I/O*	*RESET STATE*	*Alternate Function Description*
1	VPP_OTP	ADI		OTP Power Supply. Must be float
10	VBAT	ADI		Power Supply
3,6,16,25	GND	GND		Connect to Ground
11	RESET	I		INPUT. Reset signal (active high). Must be connected to GND if not used
2	P0_2/ADC2	DIO	I-PD	INPUT/OUTPUT with selectable pull up/down resistor. General purpose I/O port bit or alternate function nodes. Contain state retention mechanism during power down.
4	P2_0	DIO	I-PD	
5	P2_8	DIO	I-PD	
9	P0_7	DIO	I-PD	
12	P0_1/ADC1	DIO	I-PD	
13	P2_1	DIO	I-PD	
14	P2_2	DIO	I-PD	
15	P2_3	DIO	I-PD	
17	P2_4	DIO	I-PD	
20	P2_9	DIO	I-PD	
21	P1_4/SWCLK	DIO	I-PD	
22	P1_0	DIO	I-PD	
23	P1_1	DIO	I-PD	
24	P1_5/SWDIO	DIO	I-PU	
7	P0_0	DIO	I-PD	They are all defined as internal SPI pins. Not for use
8	P0_6	DIO	I-PD	
18	P0_5	DIO	I-PD	
19	P0_4	DI	INPUT	P0_4 & Sleep_Control_Input_Pin： Input High: Force active Input Low: Sleep allowed

4.2.Reference Design

The most recent schematic and design example, bill of material, and layout file are available from original developer . Contact us for details.

Figure 1: Module Reference Design



Circuit Description

1:VBAT supply voltage value is 2.35V~3.60V.

2:PIN1 is OTP burn enable interface, must float.

3:PIN2 and PIN12 multiplex ADC function

4:The PLBD5EITO is TTL level, The Uart port can communicate directly with the 3.3V MCU.

5:P1_X and P2_X GPIOs can multiplex use for SPI /PWM/I2C port.

6:Reserve JP1 burning interface if the PCB board has enough space.

Section A

7:PIN11 is Module reset (active high) ,keep floating if the user not use.

8:PIN19(DL_P0_4_T) is defined as sleep wakeup PIN.

Keep PIN19 external pull-up if the user dose not need low power mode.

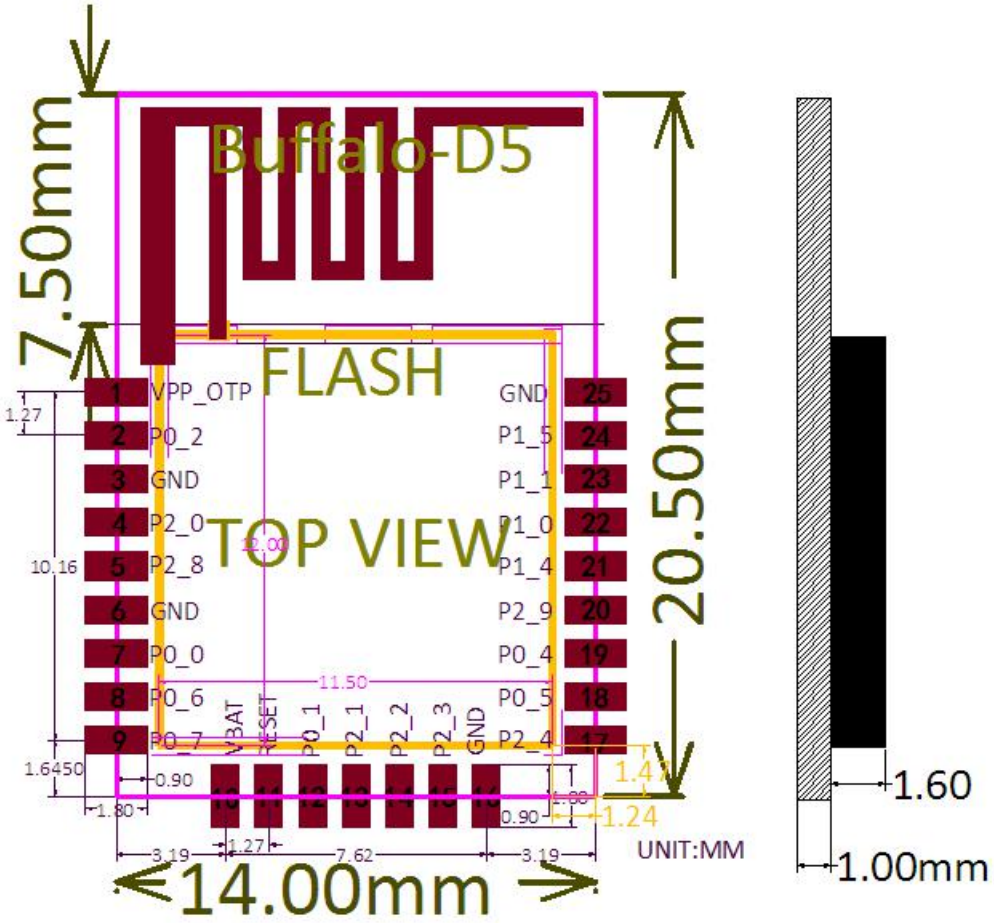
Section B

9:P0_0/P0_6/P0_5 are not for users.

4.3.Appearance and Dimensions

Figure 2 shows the size of the module.The components and prominent structure are not allowed put in this size range(20.5mm*14.0mm*2.60mm).

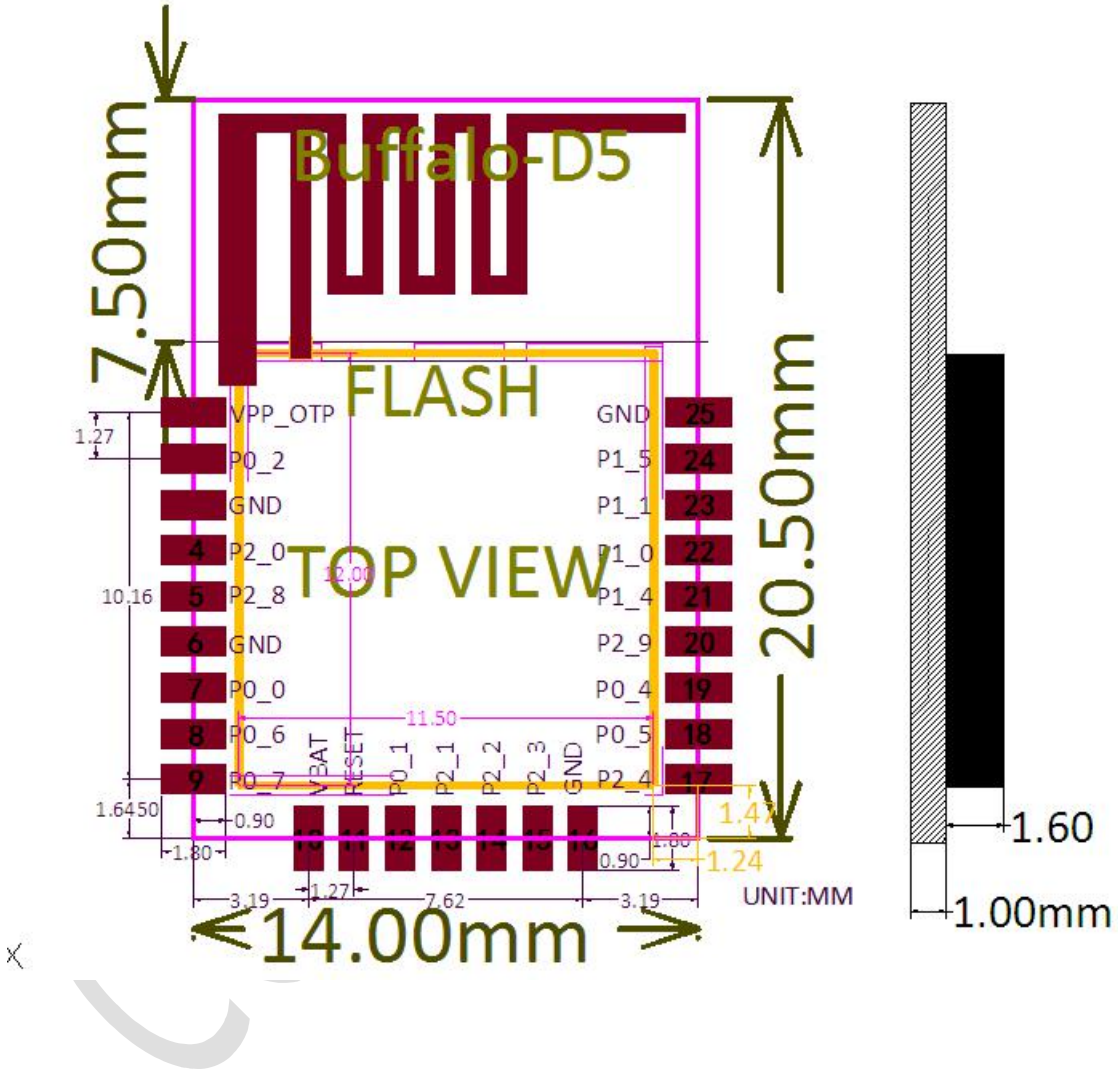
Figure 3: Module Appearance



4.4.Recommended Land Pattern

The following land pattern size is recommended for user board design. However, user can modify it according PCB soldering conditions. Sufficient examination is necessary if use the modified land pattern.

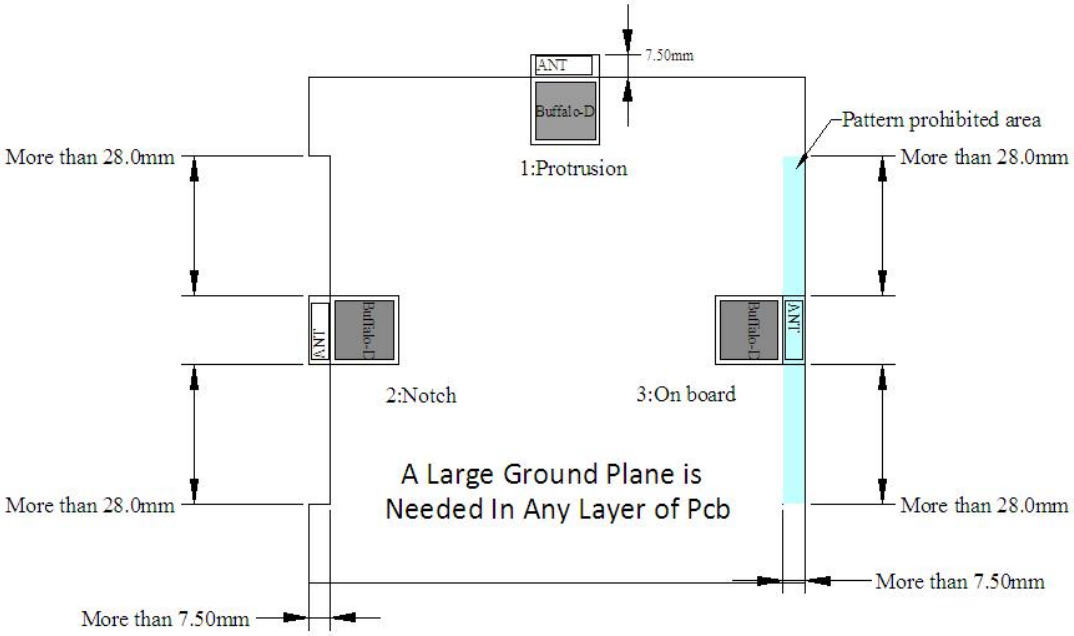
Figure 3: Mechanical Information



4.5.Module Layout Guideline

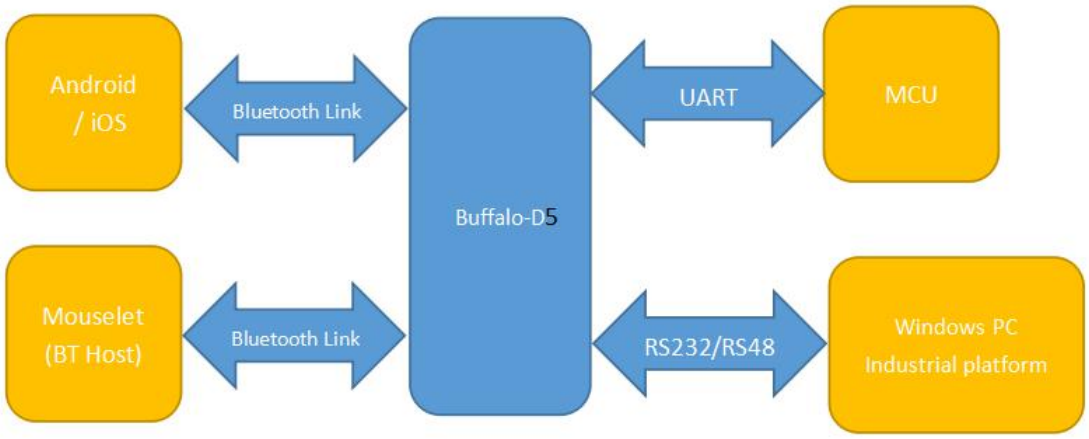
The layout on user PCB should be designed according to the following guidelines.

Figure 4: Module Placement



5. Application Diagram

Figure 5: Application Diagram



PLBD5EITO can build BT link with Android/IOS devices ,also can build a connection with Pairlink another BT module device called Mouselet.

PLBD5EITO can be accurate pass-through the data between the MCU and wireless device.

PLBD5EITO also can pass-through the data from Windows Serial-232 or Industrial Serial-485 device .

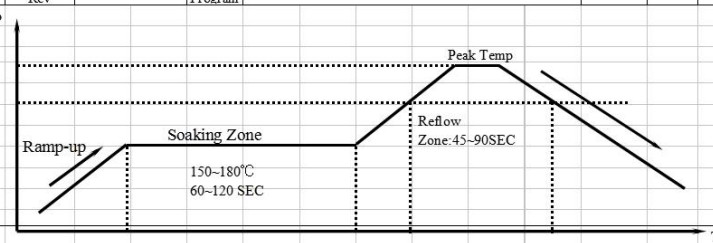
6. Welding Declare

Figure5: Standard Operation Procedure (SOP)

作 业 指 导 书
Standard Operation Procedure (SOP) -- Bufflao-D5

批准	审核	作成	作成日

生产工段 Station	SMT						工序名 Station	Reflow soldering							
文件编号 Doc No.	MSOP-FL-RX1060N-G01		版本 Rev	A0			程序名 Program	003-RR-T-S606-S3							



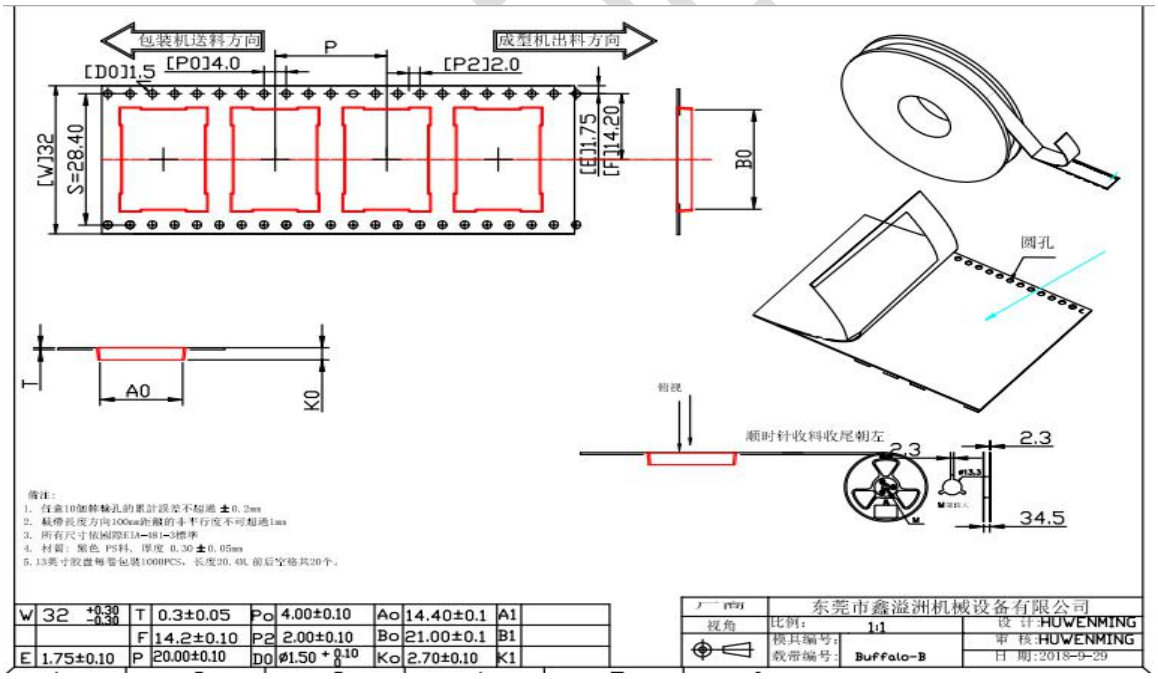
作业图

项目		Zone	1	2	3	4	5	6	7	8	9	10			
温区参数		Top	150	150	180	180	180	195	210	240	250	240			
		Bottom	150	150	180	180	180	195	210	240	250	240			
		Conveyor speed	900	mm/min											

曲线参		峰值温度	浸温	熔锡温度	上升斜率	回焊斜率	降温斜率
	Temp Range	240±5	150--180	217	25-150		183
	Time ,		60--120S	45－90S	1--3 ℃/s	1－3 ℃/s	≤4℃/s

7.Packing Information

Figure6:Rolling information



Product name	MOQ	Packing method	Single package quantity
PLBD5EITO	1000PCS	Tape and Reel	1000PCS