PLTBEITO Specification

Version	Note	Date
V1.0	Create	2018/09/28
V1.1	Modify the shape of module	2018/11/09
V1.2	Redefine PWM Port	2018/12/20
V1.3	Redefine PWM Port and ADC Port Add Power on Reset Sequence	2019/01/07
V1.4	Redefine Electrical Specification	2019/03/28
V1.5	Add Packing Information	2019/05/17
V1.6	Add Certification Information	2020/01/03
V1.7		2020/12/28

Contents

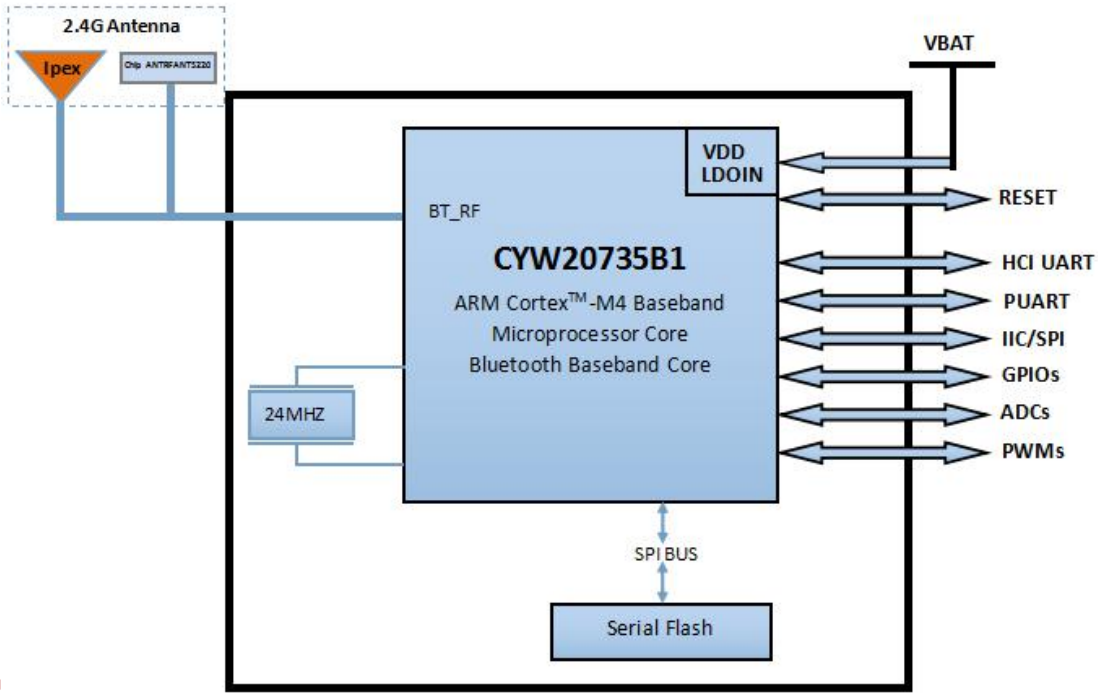
1.Functional Characteristics

PLTBEITO is SOC module developed based on the Bluetooth 5 standards. the internal integration architecture ARM® Cortex®-M4 processor.It has the advantage of small volume, low power consumption, long distance transmission, strong anti-jamming capability, low cost.Specifically applied to Bluetooth low power control area,and suitable for various occasions short distance wireless communication.

PLTBEITO integral compact, simplifies the design in hardware and institution for user. The module interface open completely to make the users has more flexible secondary development space.

The module includes 24Mhz Crystal and 8Mb SPI flash. The module also integrated with Ipex connector and ceramic antenna.users can better the expansion of the RF performance.Circuit block diagram of the module is shown in Figure 1.

Figure 1: PLTBEITO Circuit Block Diagram



1.1.Product Feature

1: PLTBEITO under Bluetooth 5 specification.
2: Supports Cypress proprietary data rate up to 2 Mbps.
3: Support SIG Mesh and Multi-link protocol.
4: Easy to extend SPI Flash.The default value is 8Mbit.Memory size is optional.
5: Integrated IPEX connector and Ceramic antenna
6: Support OTA function.

1.2. Main Application Domain

1: Home automation / Intelligent access control system.
2: Industrial telemetry / Industrial data collection.

2.Electrical Specifications

- Integration architecture ARM® Cortex®-M4 processor
- 320KB RAM,2MB ROM, 64KB Patch RAM, 8Mbit Flash
- Include 8Mbit SPI FLASH, Memory size is optional
- Supports Cypress proprietary data rate up to 2 Mbps
- Supports Generic Access Profile (GAP)
- Supports Adaptive Frequency Hopping (AFH)
- RF Frequency:2400MHz ~ 2483.5 MHz
- Channel Spacing:2MHz
- Channel Center Frequency:2402MHz~2480MHz
- Modulation:GFSK

2.1.Absolute Ratings

Parameter	*Specification*			*Unit*
	Min.	*Typical*	*Max.*	
Power Supply	-0.3	-	+3.8	V
Current Consumption	-	-	30	mA
Storage temperature	-40	-	+150	℃
Working temperature	-30	-	+85	℃
ESD HBM	-2K	-	+2K	V
ESD CDM	-500	-	+500	V
Latch-up	-	200	-	mA

2.2.Recommended Operating Conditions

Parameter	*Specification*			*Unit*
	Min.	*Typical*	*Max.*	
Power Supply	2.7	3.3	3.6	V

Digital I/O Characteristic

Characteristics	*Symbol*	*Specification*			*Unit*
		Min.	*Typical*	*Max.*	
Input Low Voltage	VIL	-	-	0.8	V
Input High Voltage	VIH	2.0	-	-	V

Output low Voltage	VOL	-	-	0.4	V
Output High Voltage	VOH	VBAT-0.4V	-	-	V

2.3.Power Consumption

Current consumption measured in BLE mode with 3.30V power on in VBAT.

Operational Mode	*Conditions*	*Typical*	*Unit*
Receiving	Receiver and baseband are both operating, 100％ON	8	mA
Transmitting	Transmitter and baseband are both operating, 100％ON	18	mA
Flash Operation	Erase and write flash	22	mA
HIDOFF(Deep Sleep)		18	uA

Current consumption measured in Pairlink connected mesh mode.

Work Mode	*Status*	*Average*	*Unit*
Mesh disable	Power on	4	mA
Discoverable	Broadcast	4.49	mA
Single mode	Home id configurated	2.66	mA
Connected	IN MESHnet	3.11	uA

Note: These data are based on the development board with Demo_SW, only for customer reference.
The actual power consumption according to the customer's application

2.4.RF Specifications

Parameter	*Conditions*	*Min.*	*Typical*[a]	*Max.*	*Unit*
Receiver RF Specifications					
Frequency range	-	2402	-	2480	MHz
RX sensitivity[b]	-	-	-91.5	-	dBm
Maximum input	GFSK,1 Mbps	-	-	-20	dBm
Transmitter RF Specifications(TBD)					
Frequency range	-	2402	-	2480	MHz
Class 1: GFSK TX power		-	10	-	dBm
Power control step	-	2	4	8	dB

a.Typical operating conditions are 3.3V operating voltage and 25°C ambient temperature.
b.The receiver sensitivity is measured at BER of 0.1% on the device interface.

3.Physical Parameters

Parameter	*Performance*	*Note*
Distance	60M	Environment: Sunny and open Antenna: Ceramic antenna, Airspeed: 1Mbps
Crystal	24MHz	Industry Standard
Protocol	BLE4.1/BLE4.2/BLE5	Supported data rates: 1 Mbps, 2 Mbps
Package	Patch	Refer to section 4.4
IC	CYW20735B1	60PIN-QFN
RAM	320KB	
ROM	2MB	
FLASH	8Mb	
Core	ARM Cortex-M4	
Dimensions	14.0mm*23.0mm*2.6mm	L*W*H
RF Interface	1:Ceramic antenna 2:Ipex Connector	1: + 2dBi 2:50ohm impedance matching

3.1.Peripheral Interface

- 1 x PUART interface with CTS/RTS
- 1 x HCI UART interface with CTS/RTS
- 1 x SPI interface with master/slave configurable
- 1 x I2C interface with master/slave configurable
- 10 x GPIOs
- 2 x ADCs input
- 6 x PWMs interface

4.Hardware design and PCB layout

4.1.Pin assignment and Pin Description[ab]

PLTBEITO Pin definition can refer to Figure 2.

Table 1:Module Pin Description

Pin Number	*Pin Name*	*I/O*	*POR State*	*Alternate Function Description*
10	VBAT	ADI	/	Power Supply
1,2,20	GND	GND	/	Connect to Ground
9	RESET	DI		INPUT. Reset signal (active Low). Floating if not used
3	UART_RTS	I,PU		RTS for HCI UART interface. NC if unused.
4	UART_CTS	I,PU		CTS for HCI UART interface: NC if unused.
5	UART_TXD	O,PU		Serial data input for the HCI UART interface.
6	UART_RXD	I		Serial data input for the HCI UART interface.
7	SPI_MISO	I		SPI Master In Slave Out. For Test.
8	P7	DIO	Floating	GPIO:P7/PUART_CTS PWM5
11	P4/PUART_RX	DIO	Floating	GPIO:P4/PUART_RX
12	P5/PUART_TX	DIO	Floating	GPIO:P5/PUART_TX
13	P6	DIO	Floating	GPIO:P6/PUART_RTS PWM4
14	P0/ADC0	DIO	Floating	GPIO:P0 ADC0
15	P1/ADC1	DIO	Floating	GPIO:P1 ADC1
16	P29/PWM3	DIO	Floating	GPIO:P29/PWM3
17	P28/PWM2	DIO	Floating	GPIO:P28/PWM2
18	P27/PWM1	DIO	Floating	GPIO:P27/PWM1
19	P26/PWM0	DIO	Floating	GPIO:P26/PWM0

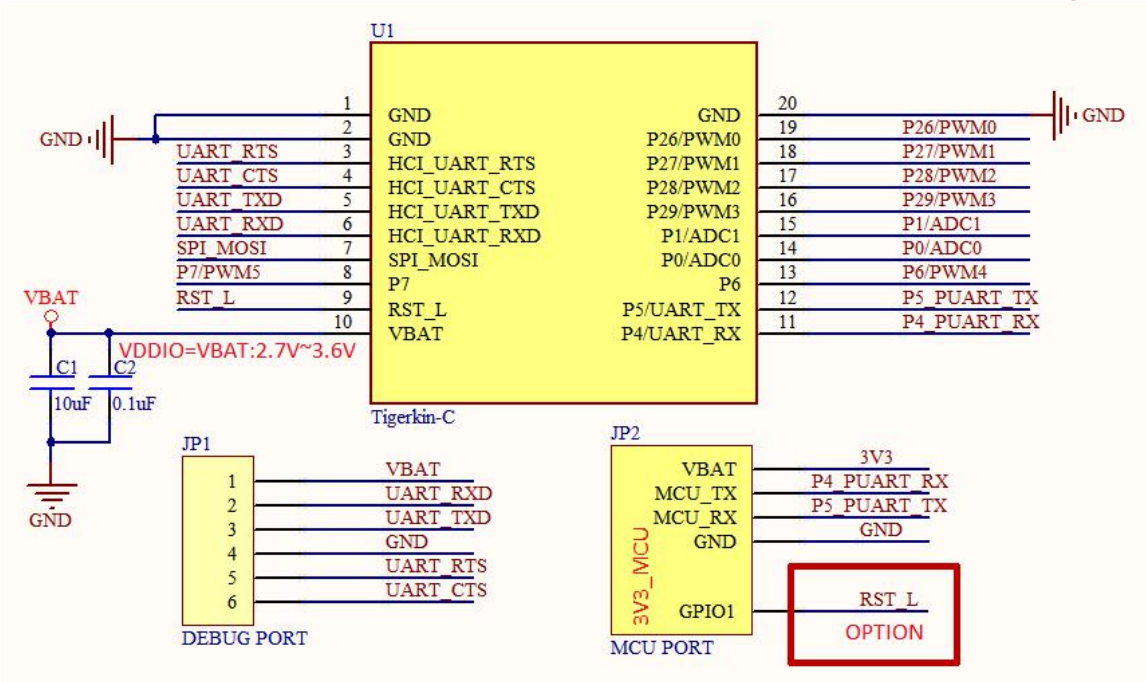
a. All GPIOs are supermux. All GPIOs can be programmed for any alternative functions. For example, key scan, SPI, I2C, IR_TX, quadrature, peripheral UART, PWM, etc.

b. During power-on reset, all inputs are disabled.

4.2.Reference Design

The latest schematic and design examples, bill of material, and layout file are available from original developer . Contact us for details.

Figure 2: Module Reference Design



Circuit Description

1:VBAT supply voltage value is 2.70V-3.60V.

2:PIN7(SPI_MOSI) reserved for testing.

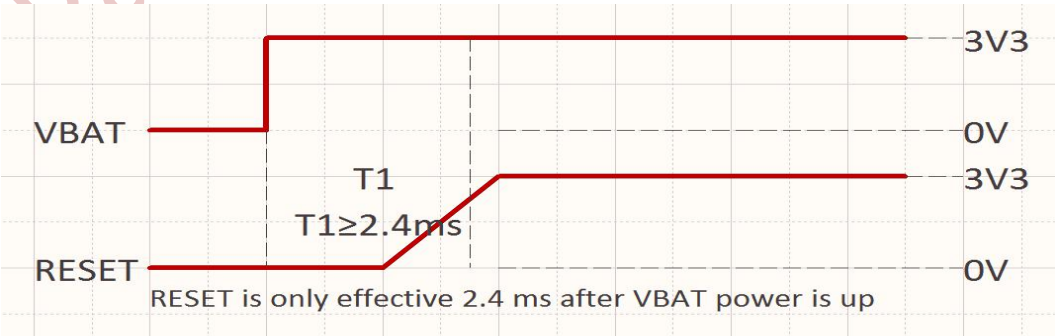
3:PIN9(RST_L) is Module Reset_Control (active Low) ,Keep floating if the user not use.

4:Reserve JP1 burning interface if the PCB board has enough space.

5:PLTBEITO support GPIOs supermux, All GPIOs can be defined as SPI /UART/I2C.

6:Only PIN14(P0) and PIN15(P1) support ADC function.

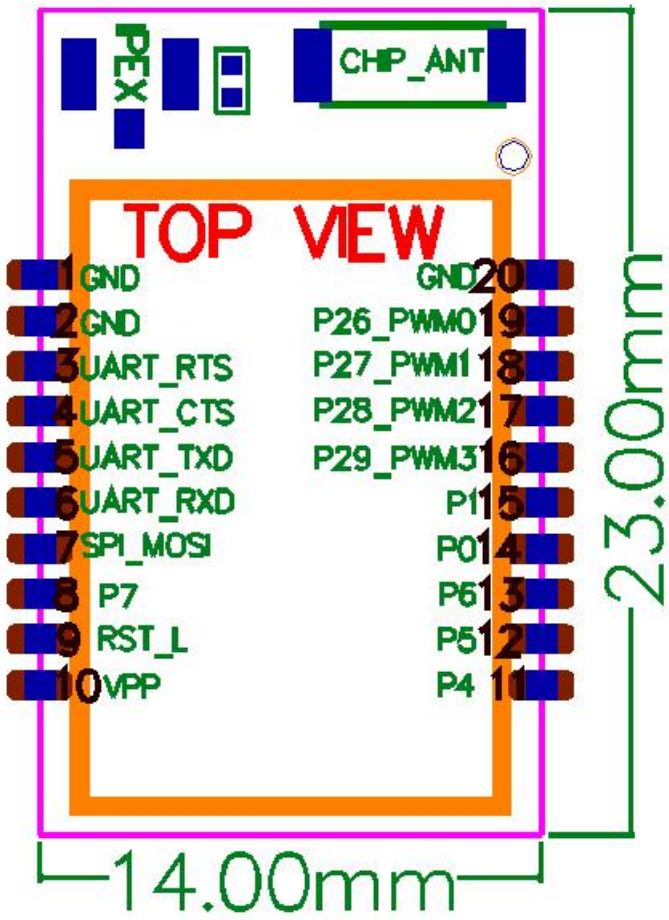
7:PLTBEITO Power on Reset sequence.



4.3.Appearance and Dimensions

Figure 3 shows the size of the module.The components and prominent structure are not allowed put in this size range(23.0mm*14.0mm*2.60mm).

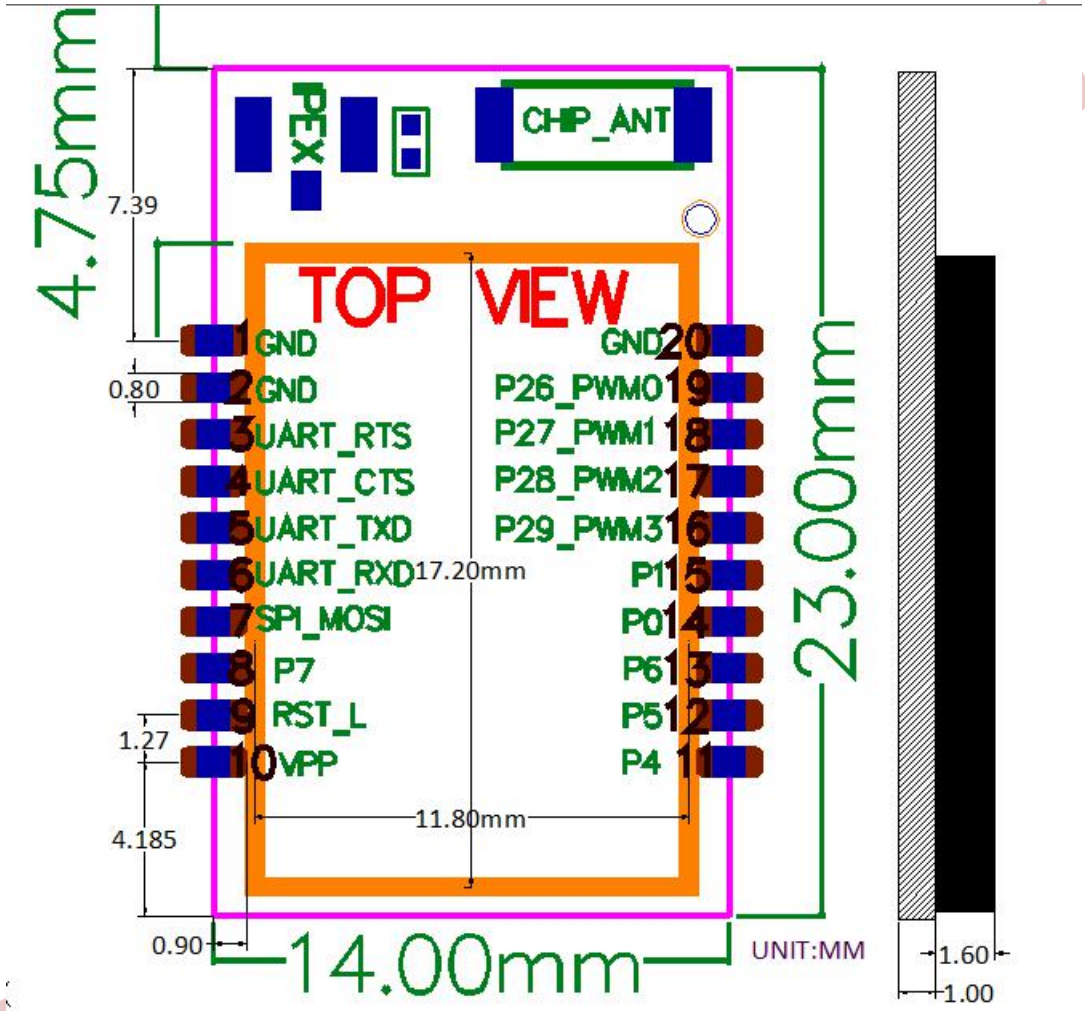
Figure 3: Module Appearance



4.4.Recommended Land Pattern

The following land pattern size is recommended for user board design. However, user can modify it according PCB soldering conditions. Sufficient examination is necessary if use the modified land pattern.

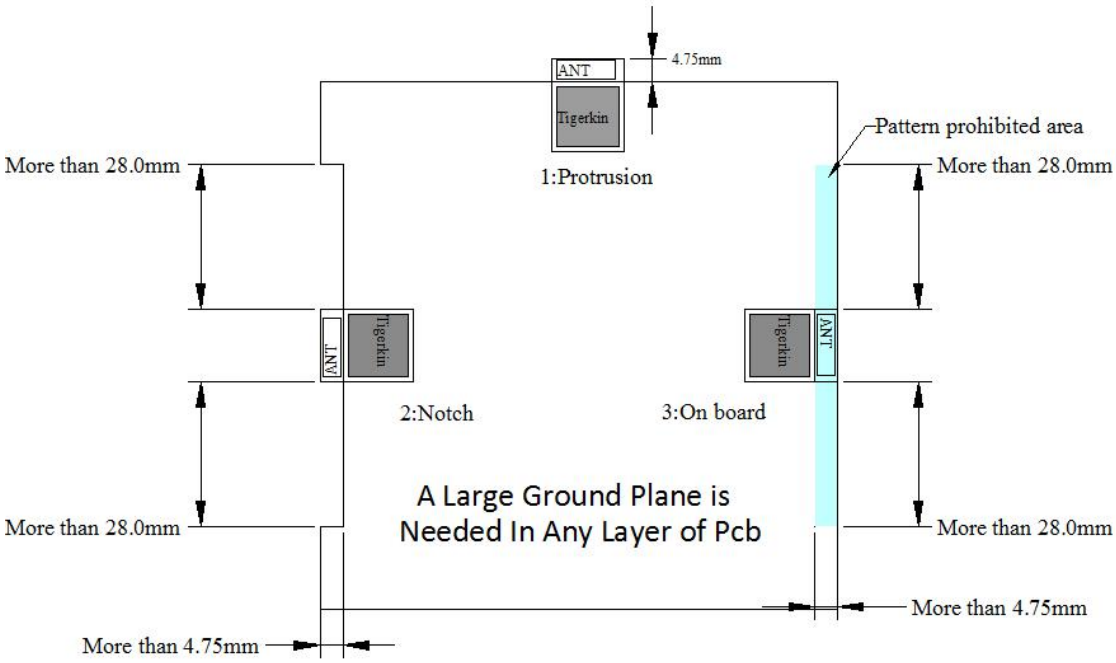
Figure 4: Mechanical Information



4.5.Module Layout Guideline

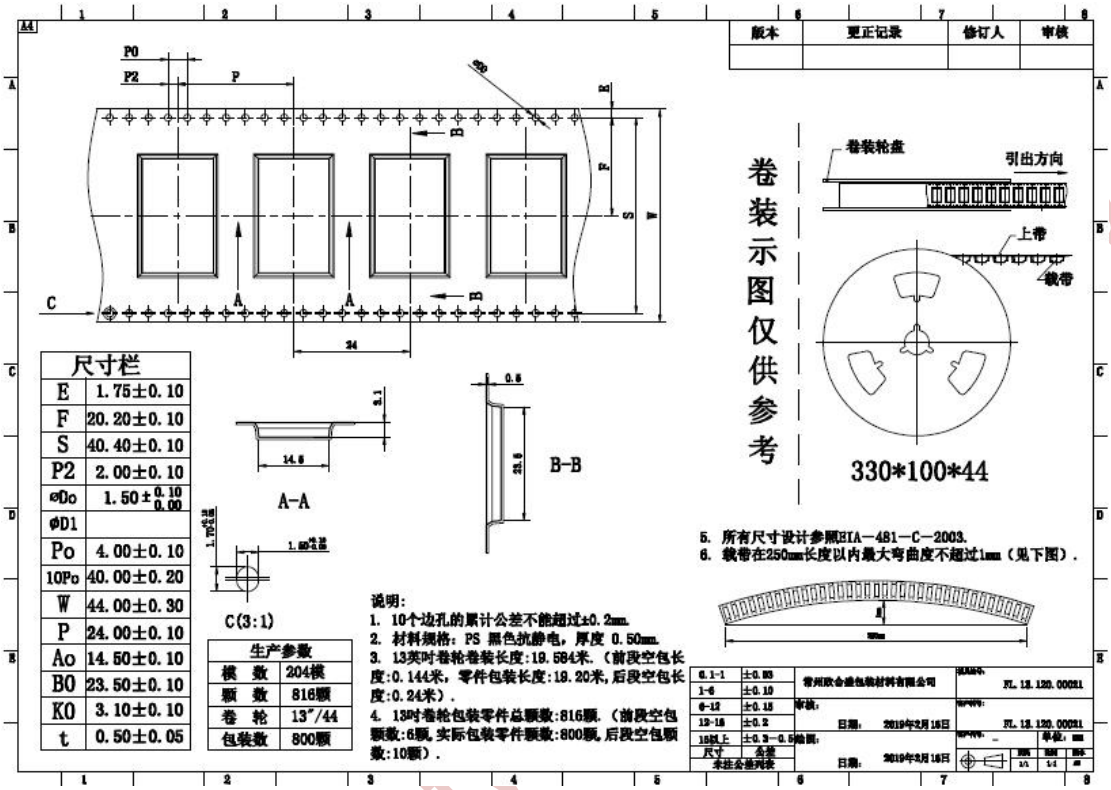
The layout on user PCB should be designed according to the following guideline.

Figure 5: Module Placement



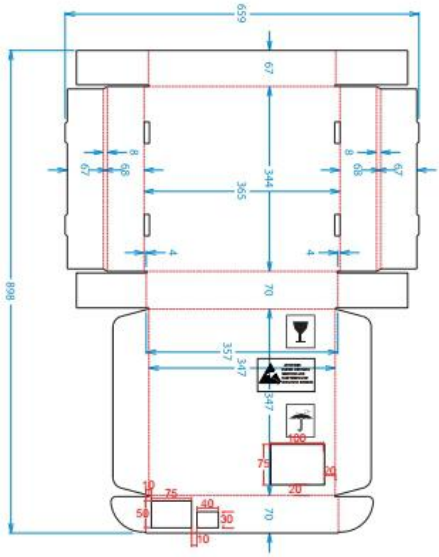
5.Packing Information

5.1.Rolling Information



Product name	MOQ	Packing method	Single package quantity
PLTBEITO	800PCS	Tape and Reel	800PCS

5.2.Master Carton Information



5.3.Label Information

A) Label on module

PLTBEITO has passed BQB\FCC\CE\IC\MIC\RoHS\SRRC certification

B) Label on vacuum bag and pizza box.

Product name	PLTBEITO
Model name	Customer Corresponding Item Number
Customer PN	Customer Part Number
Quantity(PCS)	800 pcs
Product date	YY.MM.DD
Product Version	SW Version
Product Type	Bluetooth Module
MFG PN	NA

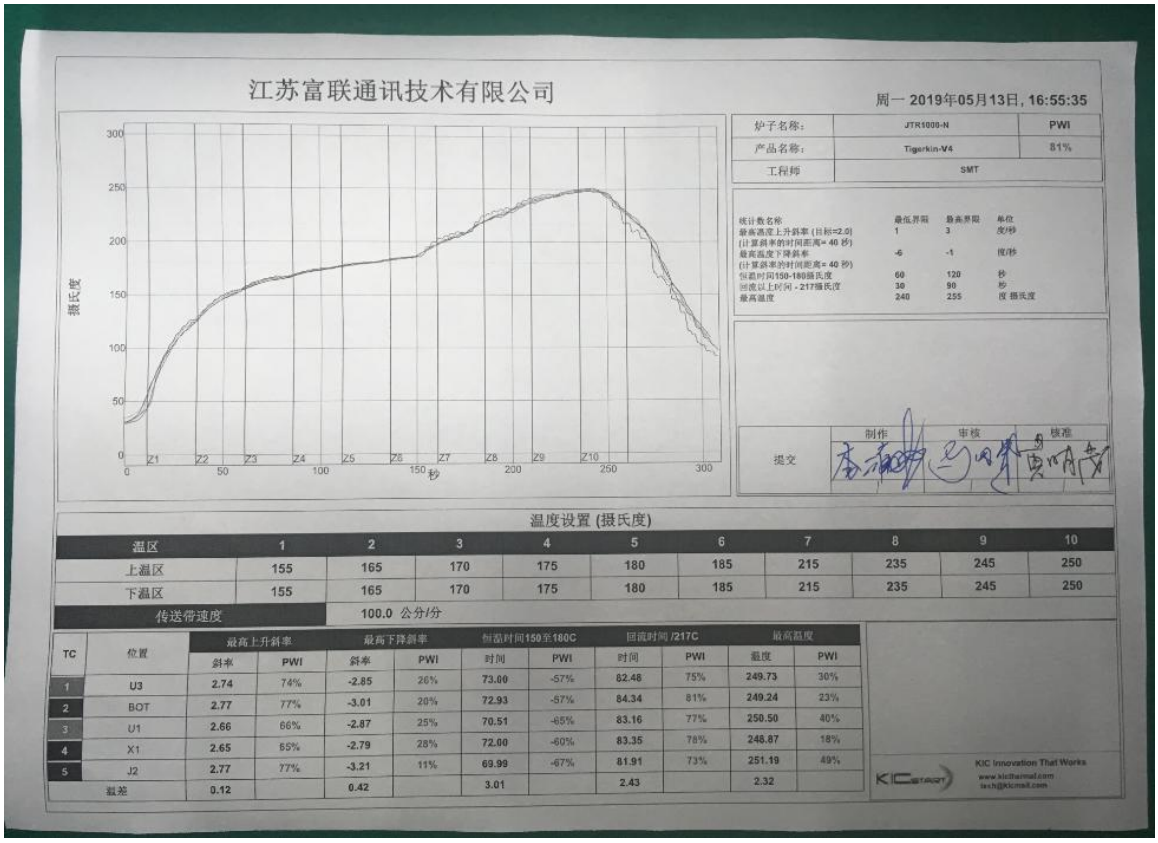
C) Label on carton

Product Name	Customer Corresponding Item Number
Customer PN	Customer Part Number
Quantity(PCS)	4000pcs
Produced date	YY.MM.DD
C/N	Cartoon Number

6. Welding Declare

The PLTBEITO module only supports one reflow soldering , and the module failure caused by multiple reflow soldering is not responsible.

Figure 6: Standard Operation Procedure (SOP)



江苏富联通讯技术有限公司

周一 2019年05月13日, 16:55:35

炉子名称:	JTR1000-N	PWI
产品名称:	Tigerkin-V4	81%
工程师	SMT	

统计数名称	最低界限	最高界限	单位
最高温度上升斜率 (目标=2.0) (计算斜率的时间距离= 40 秒)	1	3	度/秒
最高温度下降斜率 (计算斜率的时间距离= 40 秒)	-6	-1	度/秒
恒温时间150-180摄氏度	60	120	秒
回流以上时间 - 217摄氏度	30	90	秒
最高温度	240	255	度 摄氏度

提交	制作	审核	核准

温度设置 (摄氏度)

温区	1	2	3	4	5	6	7	8	9	10
上温区	155	165	170	175	180	185	215	235	245	250
下温区	155	165	170	175	180	185	215	235	245	250
传送带速度	100.0 公分/分									

TC	位置	最高上升斜率		最高下降斜率		恒温时间150至180C		回流时间 /217C		最高温度	
		斜率	PWI	斜率	PWI	时间	PWI	时间	PWI	温度	PWI
1	U3	2.74	74%	-2.85	26%	73.00	-57%	82.48	75%	249.73	30%
2	BOT	2.77	77%	-3.01	28%	72.93	-57%	84.34	81%	249.24	23%
3	U1	2.66	66%	-2.87	25%	70.51	-65%	83.16	77%	250.50	40%
4	X1	2.65	65%	-2.79	28%	72.00	-60%	83.35	78%	248.87	18%
5	J2	2.77	77%	-3.21	11%	69.99	-67%	81.91	73%	251.19	49%
温差		0.12		0.42		3.01		2.43		2.32	

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